REMARKS/ARGUMENTS

Reconsideration of this application is requested. Claims 1-36 remain in the application, with claims 1-3, 7-9 13-17, 21-25 and 27-36 having been amended. New claims 37-46 have been added. Independent claims 1, 7, 15, 21, 29, 31, 33 and 35 have been amended to include an internal matrix and an output matrix. The internal matrix and output matrix are described in the specification in paragraphs [0175] and [0176]. Claims 2, 3, 8, 9, 13, 14, 16, 17, 22, 23, 27, 28, 30, 32, 34 and 36 have been editorially amended to conform the amended independent claims from which they depend. Claims 24 and 25 have been amended to depend from claim 23.

New claim 37 includes writing a plurality of bits of the digital signal to an internal matrix in a convolutional interleaver, wherein the plurality of bits are arranged in a plurality of interleaver partitions, reading the bits from the internal matrix, and mapping bits from the interleaver partitions to frequency partitions in a radio signal. The convolutional interleaver with interleaver partitions is described at several locations in the specification, for example, in paragraphs [0166] to [0168]. Mapping bits from the interleaver partitions to frequency partitions in a radio signal is described at several locations in the specification, for example, in paragraph [0183].

The assignment of rows to the frequency partitions of new claim 38 is described in the specification in paragraph [0183].

The mapping of each row of bits to one of the frequency partitions as a complex vector of new claim 39 is described in the specification in paragraph [0183].

The sequential processing of the rows of bits of new claim 40 is described in the specification in paragraph [0187].

The use of control data sequence bits that are mapped to a reference subcarrier in the radio signal of new claim 41 is described in the specification in paragraph [0183].

The non-sequential addressing scheme of claim 42 was contained in original claim 1.

Processing a row of bits in the matrix for each symbol in the orthogonal frequency division multiplexed signal of claim 43 is described in the specification in paragraph [0187].

The plurality of bits of the digital signal comprising channel coded transfer frames of new claim 44 is described in the specification in paragraph [0148].

The elements of new claim 45 are described in the specification in paragraph [0186].

The elements of new claim 46 are described in the specification in paragraph [0188].

In Section 2 of the Detailed Action portion of the Office Action, claims 1-13, 15-27 and 29-36 have been rejected under 35 U.S.C. 102(e) as being anticipated by Prasad (6,748,561).

Regarding claims 1-5, 7-11, 15-19, 21-25 and 29-36, Prasad was cited as showing in figures 1A-4, a method and apparatus for transmitting and receiving the digital data comprising interleaving (Fig. 2A) and de-interleaving (Fig. 2B) the digital signal, wherein the writing and reading functions of interleaving and de-interleaving are performed in a non-sequential addressing scheme.

This rejection is traversed. The Applicant respectfully submits that the amended claims contain features that are neither disclosed nor suggested by Prasad. In particular, each of the independent claims 1, 7, 15, 21, 29, 31, 33 and 35 includes an internal matrix and an output matrix, wherein at least one of the steps of writing and reading to or from the internal matrix follows a non-sequential addressing scheme.

The present invention relates to convolutional interleavers that use a non-sequential addressing scheme. As discussed in the application in paragraph [0167], when the total number of bits being interleaved is greater than the transfer frame size, an additional matrix is used to manage the data flow. A convolutional interleaver can be implemented without the need for block synchronization information that is required in a block interleaver. The Applicant respectfully submits that Prasad does not disclose or suggest a convolutional interleaver or an interleaver having an internal matrix and an output matrix. Prasad specifically teaches away from the use of separate internal and

output matrixes by providing an interleaving scheme that uses a single memory buffer, see the Abstract, and column 3, lines 57-58.

The dependent claims include additional features that are not disclosed or suggested by Prasad. For example, claims 3-5, 9-11, 17-19, 23 and 25 refer to partitions in the internal matrix.

Regarding claims 6, 12, 20 and 26, the Office Action states that Prasad does not explicitly disclose scrambling the bits; however according to the Office Action, it was considered to be an inherent function of interleaving to scramble the input bits during the operation. Since claims 6, 12, 20 and 26 depend from claims 1, 7, 15, and 21 respectively, this rejection is traversed for the reasons set forth above with respect to the traversal of the rejection of claims 1, 7, 15, and 21, and for the following reasons. While the interleaving function can be considered to scramble bits that are output from an interleaver, claims 1, 7, 15, and 21 specify that the bits in the internal matrix are scrambled. The Applicant respectfully submits that scrambling bits that are input to an interleaver is not an inherent function of an interleaver.

Regarding claims 13 and 27, Prasad was cited as further teaching channel coding the bits before interleaving. Since claims 13 and 27 depend from claims 7 and 21 respectively, this rejection is traversed for the reasons set forth above with respect to the traversal of the rejection of claims 7 and 21.

In Section 4 of the Detailed Action portion of the Office Action, claims 14 and 28 have been rejected under 35 U.S.C. 103(a) as being unpatentable over Prasad (6,748,561) in view of Dent (6,944,206). Prasad was cited as teaching the subject matter claimed except for scrambling the bits before writing the bits to the matrix. However, Dent was cited in the Office Action as teaching scrambling the bits before interleaving (writing). According to the Office Action, it was considered to have been obvious to one of ordinary skill in the art at the time the invention was made to modify the system of Prasad by employing the teaching of Dent so that the more robust signals and protection against noises can be achieved.

Since claims 14 and 28 depend from claims 7 and 21 respectively, this rejection is traversed for the reasons set forth above with respect to the traversal of the

rejection of claims 7 and 21, and for the following reasons. While Dent mentions the use of scrambled bits, the Applicant respectfully submits that Dent does not appear to show scrambling of bits before interleaving. In addition, there is nothing in the record to indicate that a combination of the teachings of Prasad and Dent would result in more robust signals and protection against noise.

All claims in the application are believed to be allowable. An early Notice of Allowance is requested.

Respectfully submitted,

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